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TECHNICAL PAPER

Are Electrical Circuit Languages Robust Enough for Photonics?

Why It is Time to Rethink Electro-Optics Co-Design

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When modeling photonics in electro-optical systems, just because something *can* be done does not mean it *should* be done. Is the design decision you make today going to limit you tomorrow as industry and customer requirements evolve? What previously worked for simple transceiver photonic ICs (PICs) is not necessarily going to work for the next generation of high-density AI and photonic computing chips. It is tempting to use electrical behavioral and circuit languages—such as Verilog-A and SPICE—for photonic design because these languages are familiar. But what will this cost you in the long run? Companies that want to deliver innovative electro-optics systems need to use simulators that incorporate electronic and photonic design capabilities.

Here's a look at why electrical circuit languages are not robust enough for electro-optics co-design, and why designers are upgrading to unified electronic-photonic design platforms that allow more natural, domain-specific characterization of electronics and photonics.

Introduction

Traditionally, chip designers for fiber-optic systems using electronic design automation (EDA) tools frequently needed a way to model a few photonic components in the same design environment with the electronics. Examples include modeling lasers or modulators with their electrical driver circuits, or modeling transimpedance amplifier (TIA) and receiver electronics with the photodetector. These designs focused primarily on optimizing electronics. Since the electronic component count is usually several orders higher than the photonic component count, it was typically sufficient to model a few photonic components through electrically equivalent circuit representations using SPICE or Verilog-A [1]. It is no surprise that when PICs picked up momentum, early electro-optical co-design approaches continued [2-5].

However, modeling is only one of the many stages in a schematic-driven layout (SDL) design flow for PICs. An electronic representation of photonics makes the entire electronic-photonic design automation (EPDA) process much more inefficient than it needs to be.

We cover the following aspects of EPDA design in this paper:

- The basics of electro-optics co-design, including the three core requirements of photonic circuit simulations and analyses: signals, models, and measurements
- How each of these three requirements differ from their electrical counterparts
- The repercussions of representing optical signals as electrical signals since this affects not only the SDL design flow for PICs, but also the ability to capture the correct physics of the circuit
- The benefits of maintaining photonic models and process design kits (PDKs) as photonic designs versus electronic designs

Basics of Photonic Circuit Simulations

The three key components in photonic circuit simulations are depicted in Figure 1. Multi-wavelength optical signals propagate in forward and backward directions to form a photonic circuit [6] that is comprised of active, passive, linear, and nonlinear photonic components.

The behavior of these photonic components is usually polarization and wavelength dependent. Optical probes are placed at the points of interest in circuit to extract performance estimates. The performance estimates have strong correlations to the presence of optical reflections and resonances in the circuit, optical crosstalk (inter- and intra-channel crosstalk, polarization crosstalk), optical phase- and intensity noise, dispersion (chromatic and polarization) and nonlinear physics of the photonic devices. In simulations that describe an optical signal as an electrical signal or model a photonic component as an electrical equivalent, there is a high risk of getting an inaccurate estimate of the circuit performance—thereby jeopardizing the commercial success of the design.

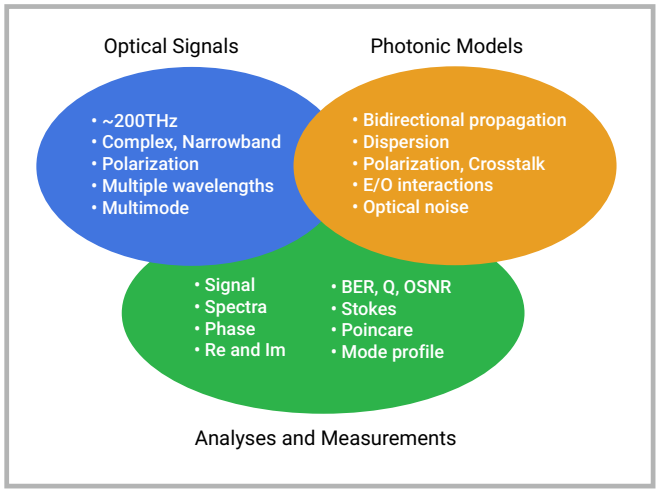


Figure 1: Optical signals, photonic models, and many of the quantities of interest are fundamentally different than in electrical circuit simulations

Optical Signals Versus Electrical Signals

Electrical signals describe current and voltage in the RF domain and are real-valued, baseband signals. A baseband signal has non-zero spectral contents near DC and is lowpass. Its Fourier transform is Hermitian and can be described by the positive frequency part of the spectrum.

Optical signals, on the other hand, are analytic, narrowband signals with a complex-valued envelope, i.e., a complex number with real and imaginary parts describing amplitude and phase modulation of the optical carrier. An optical signal is typically represented with the complex envelope and its center frequency as two distinct pieces of information. The optical carrier can be a single-wavelength or a multi-wavelength signal propagating with polarization states and transverse mode profiles. Since there isn't an equivalent of these optical signal attributes in the electrical domain, representing an optical signal electrically requires assigning multiple electrical signals and pins to each of the signal properties and the propagation direction. Figure 2 depicts this mapping.

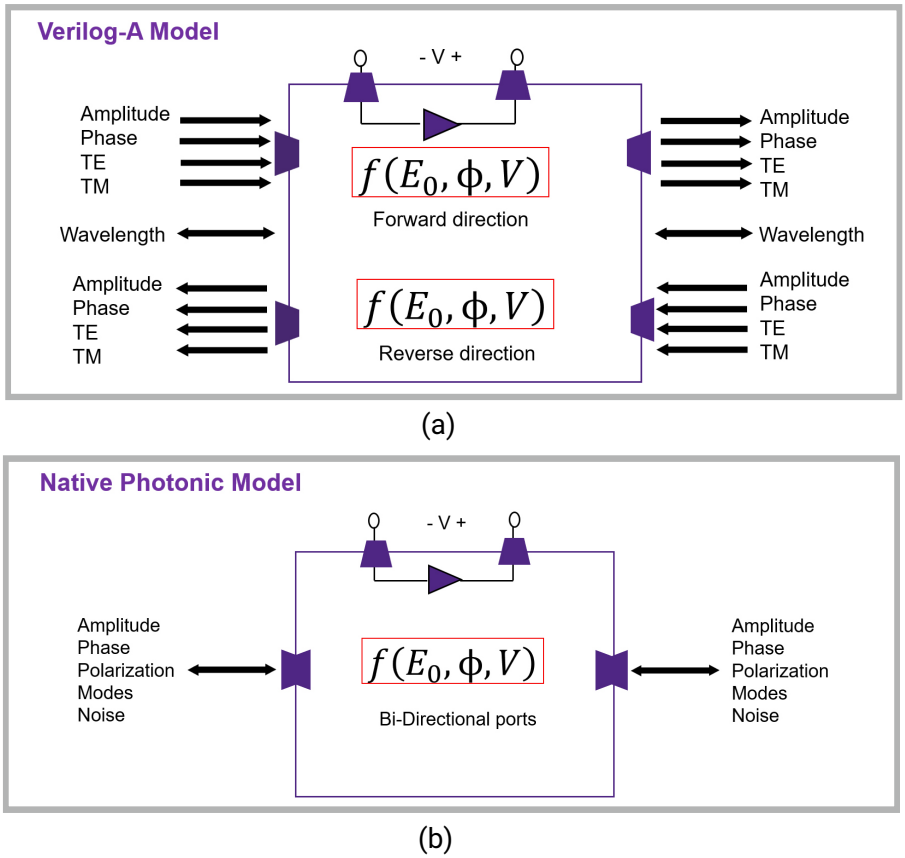


Figure 2: Representing an optical signal in electrical domain requires up to a nine-fold increase per wavelength in the number of electrical ports and signals for every photonic device in the circuit

Optical Connectivity as Electrical Buses

Even when multiple electrical signals (mapping the various properties of the optical signal) can be collectively represented as buses, multiwavelength and multimode photonic devices can dramatically increase the signal and pin count. This creates serious challenges for tracking, connecting (crossings, for example), and probing signals at the pin or bus levels.

In addition, the likelihood of layout-vs-schematic check (LVS) violations dramatically increases and jeopardizes productivity and time to market. Some may argue that current generation of photonic circuits and devices are mostly singlemode and therefore operate at one to a very few wavelengths. This assumption not only ignores the application areas of PIC technology where the hypothesis falls apart— like DWDM, sensing or bio-photonics— but also provides no compatibility with future advancements.

Kirchhoff's Formalism and Photonic Circuits

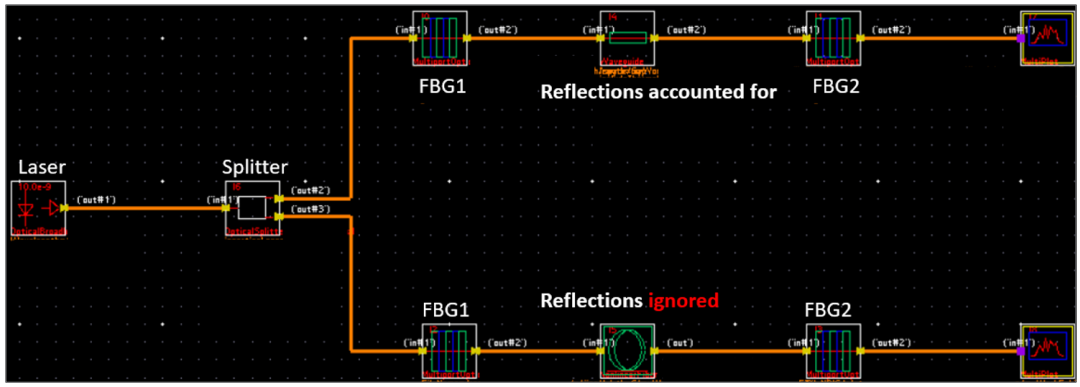
Electrical circuit simulators for analog electronics are based on modified nodal analysis and Kirchhoff's electrical circuit laws [7-8]. The vectoral nature of optical field waves and multiple orders of reflections in photonic circuits due to neighboring photonic components results in coherent multi-path interference (MPI).

Modeling these effects in the electrical domain using Kirchhoff's voltage and current (both scalar quantities) conservation laws results in unintuitive, time-consuming complexities to PDK development and design. It's no surprise that foundries and PIC designers using Kirchhoff's formalism for photonics often choose to ignore these critical impairments. As we will discuss next, overlooking MPI can lead to inaccurate predictions of PIC behavior that increases the risk of unsuccessful designs and lower yields.

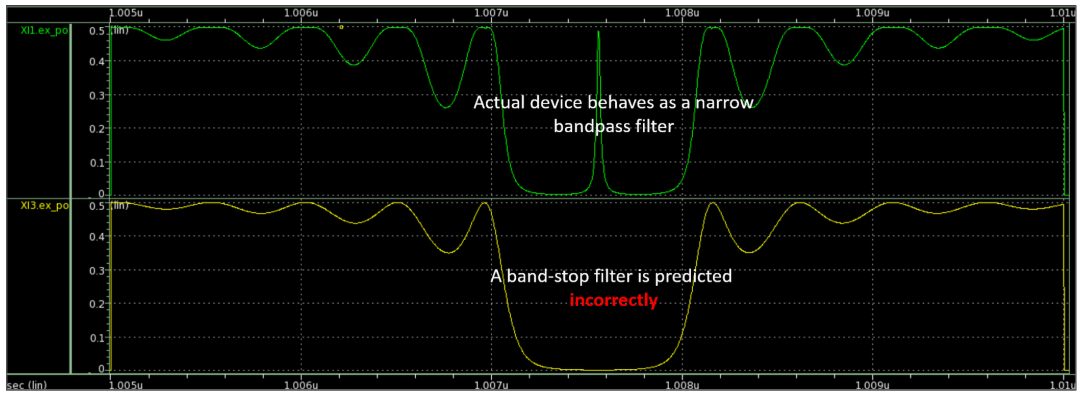
Approximations Are Expensive

Many photonic model libraries implemented in Verilog-A or SPICE do not account for bidirectional signal propagation (such as reflections) and device nonlinearity. Some implementations only account for device behavior one wavelength or one polarization at a time, which overlooks important physical properties such as dispersion, polarization crosstalk, and crosstalk from neighboring wavelengths.

As an example of the cost of ignoring reflections, consider the simple design example shown in Figure 3, which includes two identical gratings separated by an optical waveguide[9]. When broadband light is applied as a source, multiple orders of coherent reflections from the gratings result in a high quality-factor narrow passband at the steady-state. If the component models or the circuit simulator do not support the modeling of reflections, the narrow passband is totally missed and a designer would mislabel the design as a band-reject filter.



(a)



(b)

Figure 3: Correct accounting for bidirectional propagation of optical signals is necessary to arrive at the right design

Treating one wavelength at a time and ignoring nonlinearities of a device can also lead to an equally misleading conclusion. As shown in Figure 4, when multiple wavelengths pass through a nonlinear photonic device at the same time, a number of additional wavelengths are generated at the device output.

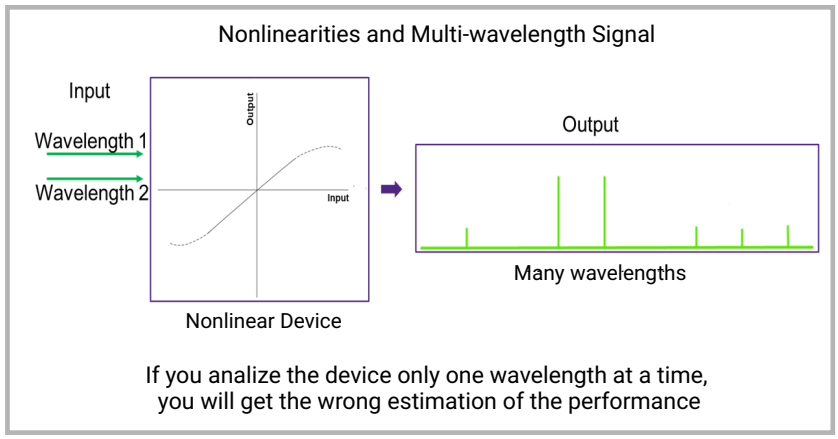


Figure 4: Analyzing a nonlinear photonic device one wavelength at a time leads to catastrophic errors because the performance is not a superposition

These additional wavelengths introduce unwanted distortions to the desired signal, which leads to an overly optimistic or incorrect performance estimate.

Overhead Costs to Consider When Creating and Maintaining PDKs

A critical part of the rapid adoption of PICs is PDK quality and maturity. Designers who use electrical PDKs are burdened with manually managing optical signal representation, port mapping, connectivity, and verification trap avoidance. In this scenario, it is easy to become frustrated by increasing component and wavelength counts. And if the electrical circuit simulator can't extract photonic quantities at the probes (such as those in Figure 1), foundries need to provide models of conversion elements to obtain this information.

If PDK data is encrypted in Verilog-A models, even simple customizations require foundry intervention. And since photonics are analog, a lot of customizations will be needed during design phases. Without detailed knowledge of how a foundry has implemented electrical mapping of optical signal attributes, designers cannot add custom components without help from the foundry. Even if such help is free as part of the foundry agreement, it nonetheless costs time and productivity.

Unlike using photonic primitives to build PDKs, writing Verilog-A models for each PDK element is not a one-time exercise. The PDK creator is responsible for accounting for parameters like dispersion, polarization dependence, bidirectional propagation, and signal mapping in the source code. For PDKs created in Verilog-A, each change to the process and technology can require code updates.

On the other hand, if photonic PDKs are built with domain-specific model primitives, revisions can be made much more easily by updating or replacing data files—and no source code changes are needed.

While new syntaxes for photonic-to-electrical port mappings are being developed by EDA vendors, multimode modeling has remained out of reach. It makes technological and financial sense to create photonic PDKs using photonic primitives—without any artificial diversions via electronics. Table 1 compares differences in the level of effort required when using photonic versus electrical simulators.

Task	Effort when using photonic circuit simulator OptSim Elite	Effort when using electrical simulators
Modeling optical reflections and bidirectional propagation	**None**—Natively supported	**High**—Writing model and simulator code to support bidirectionality
Creation of model library	**Normal**—Supplied photonic primitives and generic models, or utilize Photonic Device Compiler	**High**—Writing and maintaining model code
Maintaining/updating PDKs	**Small**—No need for new schematic, just update/replace data files	**Medium**—Updating/rewriting model code
Letting designers add custom devices	**Small**—Photonic Device Compiler with Custom PDK Utility	**High**—Not possible without foundry's help
Analyzing simulation results	**None**—All analysis is provided	**High/Impossible**—Adjust simulation and analysis environment
Enabling SDL with photonic pins and wires	**None**—Natively supported in OptoCompiler™	**High**—Account for optical signal representation, ports, bus, connectivity, etc.

Table 1: ROI summary for photonic PDKs supplied in photonic vs. electronic formats

Electro-Optical Co-Design in a Seamless Simulation Environment

The photonic simulation industry has matured over the last two decades. The days are long past when co-design was possible only in electrical simulators with photonics modeled as electronics. In a modern EPDA platform such as the Synopsys OptoCompiler solution[10], co-design of electronics and photonics is seamless. OptoCompiler's simulation and analysis environment (SAE) analyzes the schematic and enables designers to choose domain-specific circuit simulators. In Figure 5, the *Design* section illustrates the process of schematic entry to co-simulation of photonic and electronic parts of a circuit using domain-specific simulators. The Synopsys OptSim™ Elite tool[11] can be used for the photonic part of the design and the FineSim®[12] and HSPICE®[13] tools can be used for the electrical sub-circuits.

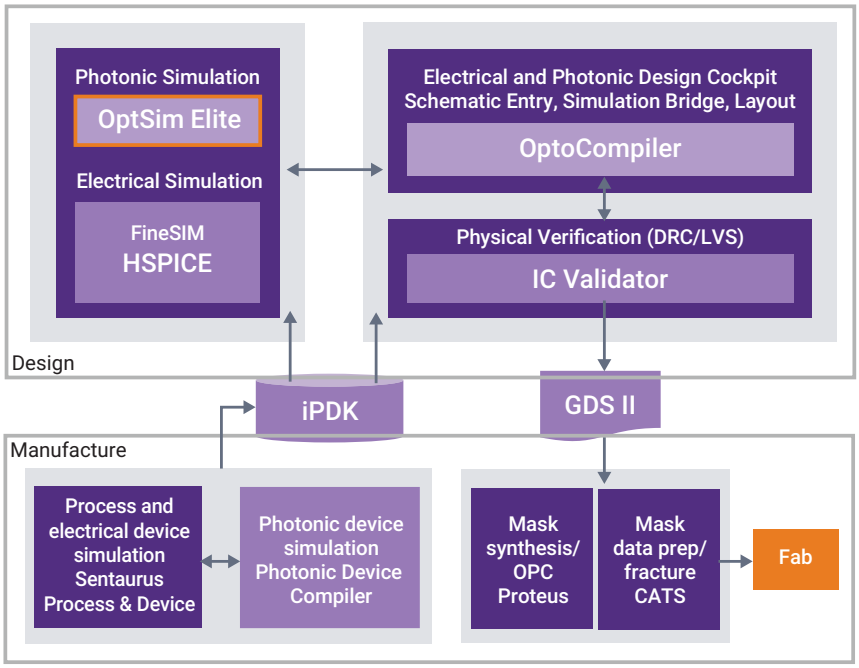


Figure 5: Complete Synopsys SDL flow including custom design and manufacture

An example of a seamless electro-optic (E-O) co-design in Synopsys OptoCompiler is shown in Figure 6. The schematic comprises photonic and electronic sub-circuits.

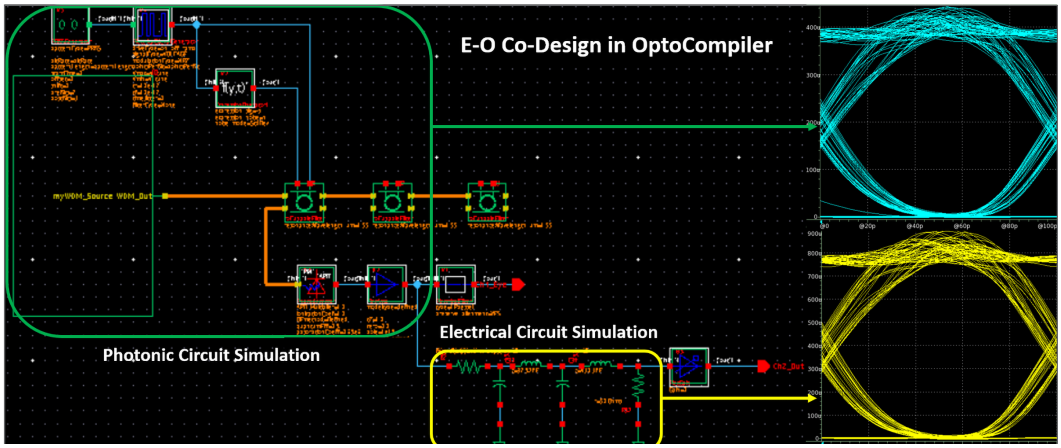


Figure 6: An illustration of E-O co-design in OptoCompiler: photonic and electronic sub-circuits are simulated in the same session by domain-specific circuit simulators OptSim Elite and HSPICE

The slowly varying envelope representation of optical signals[14] eliminates the need for terahertz rate sampling. Therefore, both optical and electrical signals can be sampled on a common grid at the modulation speeds—in the same simulation session—without additional computational overheads.

Summary

While familiarity with electrical circuit simulators may make it tempting to model photonics as electronics, it is not the most efficient path for electro-optical co-design in modern PICs. The cost of developing, maintaining, and using photonic PDKs as Verilog-A or SPICE circuits is just too high. From the designer's perspective, the approach is out of date, potentially less accurate, not scalable to future needs, and too rigid. Simulators for modeling electronics and photonics are mature today in their respective domains. The only sensible way forward for the industry is to let electronics be electronics and photonics be photonics.

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Reference

1. E. Kononov, "Modeling photonic links in Verilog-A," Master's Thesis, MIT, June 2013.
2. P. Martin, F. Gays, E. Grellier, and S. Menezo, "Development of Verilog-A models for silicon photonics devices and implementation in a standard EDA environment," MOS-AK Workshop, Présentation PowerPoint (mos-ak.org), March 28-29, 2014.
3. C. Sorace-Agaskar, J. Leu, M. Watts, and V. Stonanovic, "Electro-optical co-simulation for integrated CMOS photonic circuits with VerilogA," Optics Express, vol.23, no. 21, Oct. 2015.
4. S. Lin, "Electronic-photonic co-design of silicon photonic interconnects," Ph D Thesis, UC-Berkeley, Fall 2017.
5. J. Leu, "Integrated silicon photonic circuit simulation," Ph D Thesis, MIT, Sept. 2018.
6. J. Patel, "OptSim Circuit: A SPICE-like photonic simulator for scalable photonic integrated circuits," https://www.synopsys.com/content/dam/synopsys/photonic-solutions/documents/whitepapers/spice-photonic-simulator-scalable-pic-wp.pdf, Oct. 2017
7. C. W. Ho, A. Ruehli, and P. Brennan, "The modified nodal approach to network analysis," IEEE Transactions on Circuits and Systems, vol. CAS-22, no. 6, pp. 504-509, June 1975.
8. M. Fiers, T. V. Vaerenbergh, K. Caluwaerts, D. V. Ginste, B. Schrauwen, J. Dambre, and P. Bienstman, "Time-domain and frequency-domain modeling of nonlinear optical components at the circuit-level using a node-based approach," Journal of Optical Society of America B, vol. 29, no. 5, pp. 896-900, May 2012.
9. J. Lumeau, V. Smirnov, and L. B. Glebovjige, "Phase-shifted volume Bragg gratings in photo-thermo-refractive glass," Optical Components and Materials V, Proceedings of SPIE, vol. 6890, 2008.
10. https://www.synopsys.com/photonic-solutions/optocompiler.html
11. https://www.synopsys.com/photonic-solutions/optocompiler/optsim-elite.html
12. https://www.synopsys.com/verification/ams-verification/finesim.html
13. https://www.synopsys.com/verification/ams-verification/hspice.html
14. OptSim Elite User Guide, Chapter 9, "Signal Types and Representations."